

WHAT WE CLAIM ARE:

1. A semiconductor device comprising:
  - a semiconductor substrate;
  - an isolation region formed in a surface layer of said semiconductor
  - 5 substrate and defining a plurality of active regions;
  - at least one gate electrode formed above a substrate surface in each active region, constituting a semiconductor element in the active region;
  - an interlevel insulating film formed over said semiconductor substrate, covering said gate electrode;
  - 10 a plurality of local interconnects formed through said interlevel insulating film and electrically connected to a region of the semiconductor element;
  - a plurality of local interconnect dummies formed through said interlevel insulating film and electrically separated from said local interconnect;
  - 15 and
  - a plurality of lower level dummies each including one of an active region dummy formed through said isolation region, a laminated dummy of an active region dummy formed through said isolation region and a gate electrode dummy formed over said active region dummy and a gate electrode dummy
  - 20 formed above said isolation region,
  - wherein each of said local interconnect dummies is disposed so that said local interconnect dummy is not connected to two lower level dummies.
2. A semiconductor device according to claim 1, wherein a width of said local
- 25 interconnect dummy is in a range from a same width as a width of said local

interconnect to twice the width of said local interconnect.

3. A semiconductor device according to claim 2, wherein said lower level dummy is the active region dummy.

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4. A semiconductor device according to claim 3, wherein said semiconductor substrate has a p-well and an n-well, the active region includes silicide layers formed over both sides of said gate electrode, and the active region dummy does not lie across a boundary between the p-well and the n-well.

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5. A semiconductor device according to claim 3, wherein said local interconnect dummy is disposed only inside an upper surface of said active region dummy.

6. A semiconductor device according to claim 2, wherein said lower level

15 dummy is the gate electrode dummy formed over said isolation region.

7. A semiconductor device according to claim 6, wherein said local interconnect dummy is formed only over an upper surface of said gate electrode dummy.

20 8. A semiconductor device according to claim 2, wherein said lower level dummy is the laminated dummy and said local interconnect dummy is not connected to two or more laminated dummies.

9. A semiconductor device according to claim 8, wherein the gate electrode

25 dummy of the laminated dummy does not extend on two or more active region

dummies.

10. A semiconductor device according to claim 1, wherein said lower level  
dummies are disposed obliquely relative to a reference layout direction of said  
5 semiconductor elements.